reconstructed, for practical purposes, from the static I_{DS}–V_{DS} curves and the small-signal model of the device. This provides an attractive alternative to deriving the information from actual large-signal measurements. The technique has been successfully applied to the design of a fixed-frequency and a broad-band varactor-tuned oscillator, yielding good agreement between predictions and experiments. In the case of the varactor-tuned circuit it has been shown, in particular, that two independent tuning elements are indeed essential if the power-bandwidth capabilities of the transistor are to be fully exploited, whereby the same arguments apply to YIG-tuned circuits.

ACKNOWLEDGMENT

The author wishes to thank H. E. Heddings for his initiative in solving a variety of unconventional and demanding circuit assembly problems, and Dr. M. Omori of Avantek, Inc., for providing the devices used in this study. The helpful comments and suggestions of B. E. Spielman, R. E. Neidert, and H. A. Willing are gratefully acknowledged.

REFERENCES

[1] Y. Mitsui, M. Nakatani, and S. Mitsui, "Design of GaAs MESFET oscillator using large-signal *S*-parameters," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 981–984, Dec. 1977.

[2] K. M. Johnson, "Large signal GaAs MESFET oscillator design," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 217–227, Mar. 1979.

[3] R. S. Tucker, "Optimum load admittance for a microwave power transistor," *Proc. IEEE*, vol. 68, pp. 410–411, Mar. 1980.

[4] C. Rauscher, "Optimum large-signal design of fixed-frequency and varactor-tuned GaAs FET oscillators," in *1980 IEEE MTT-S Int. Microwave Symp. Dig.*, May 1980, pp. 373–375.

[5] C. Rauscher, "Broadband varactor-tuned GaAs FET oscillator," *Electron. Lett.*, vol. 16, pp. 534–535, July 1980.

[6] K. Kurokawa, "Some basic characteristics of broadband negative resistance oscillator circuits," *Bell Syst. Tech J.*, vol. 48, pp. 1937–1955, 1969.

[7] R. A. Pucel, R. Bera, and D. Masse, "Experiments on integrated gallium-arsenide FET oscillators at *X*-band," *Electron. Lett.*, vol. 11, pp. 219–220, May 1975.

[8] C. Rauscher and H. A. Willing, "Design of broadband GaAs FET power amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, pp. 1054–1059, Oct. 1980.

[9] C. Rauscher and H. A. Willing, "Simulation of nonlinear microwave FET performance using a quasi-static model," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 834–840, Oct. 1979.

[10] R. J. Wenzel, "Printed-circuit complementary filters for narrow bandwidth multiplexers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-16, pp. 147–157, Mar. 1968.

[11] J. R. Anderson, M. Omori, and H. F. Cooke, "A unique GaAs MESFET for low noise application," in *1978 IEDM Tech. Dig.*, Dec. 1978, pp. 133–135.

[12] D. Mawhinney, "Single-oscillator wideband VCO," Naval Electronic Systems Command, Final Rep., Contract N00039-77-C-0271, Apr. 1978.

[13] C. Rauscher and H. J. Carlin, "Generalized technique for designing broadband varactor-tuned negative resistance oscillators," *Int. J. Circuit Theory Appl.*, vol. 7, pp. 313–320, July 1979.

10-GHz 10-W Internally Matched Flip-Chip GaAs Power FET's

YASUO MITSUI, MICHIHIRO KOBIKI, MANABU WATAZE, KAZUAKI SEGAWA, MUTSUYUKI OTSUBU, AND TAKASHI ISHII

***Abstract*—A newly developed internally matched configuration for a flip-chip GaAs power field effect transistor is presented. In this structure, gate and drain electrodes of the FET chips are directly connected to the lumped dielectric capacitors in the matching networks by thermocompression bonding using no wire. A power output of 10 W with 3-dB gain and a power added efficiency as high as 14 percent has been realized at 10 GHz.**

Manuscript received May 20, 1980; revised November 26, 1980. A condensed version of this paper has been presented at the 1980 IEEE MTT-S International Microwave Symposium, Washington, DC.

The authors are with LSI Research and Development Laboratory, Mitsubishi Electric Corporation, 4-1 Mizuhara, Itami, Hyogo, Japan.

I. INTRODUCTION

RECENT advances in GaAs field effect transistor technology have steadily improved the power output and power gain capabilities of the device over the frequency range from *S*- to *Ku*-band [1]. Nowadays, solid-state power GaAs FET amplifiers are extensively used in telecommunication and phased array radar systems [2], [3]. High power output levels in the *X*-band frequency range are demanded for these applications.

For obtaining higher power output, various types of

0018-9480/81/0400-0304$00.75

power FET structures have been developed. The crossover structure [4], [5] minimizes the number of bonds required to assemble a large device with increased gate width and it gives 20 W at 8 GHz [6]. The processing, however, is complex and additional parasitics are involved in the capacitance at the crossover. The multiple bond structure, in which a large number of chips are connected with bonding wires, allows a simple processing technology and 18.5 W at 4 GHz has been obtained [7]. Device assembly, however, is complex and can have increased parasitics in very large devices. The flip-chip approach introduced by RCA [8] gives very low parasitic source inductances and low thermal resistance, but it is considerably difficult to construct a very large device because this structure requires gate and drain bonding wires.

More than 10-W CW power output has not been realized at *X*-band to date with these types of the power FET structures because of the disadvantages of each structure. On the other hand, a structure with flip-chip mounting for all three terminals and no bonding wire are expected to be more favorable for increasing power output at frequencies above the *X*-band because of minimized parasitics, good heat dissipation, and simple device assembly [9].

The most important problem left to be solved for further improvement of the FET is to achieve increased gate width without serious degradation of high-gain performance. It is well known that the internal matching technique using lumped elements is a very useful approach for realizing a large gate width device which has a low input/output impedance [10]. With our internally matched flip-chip FET's developed earlier, the electrical distance from the chips to the matching network was too large. The associated series inductance, especially for the input, however, has been found to be one of crucial problems for increasing the operating frequencies of the FET to *X*-band.

We have overcome this problem by developing a unique internal matching configuration. Gold plated gate and drain metal posts are directly connected to the electrodes of the dielectric lumped capacitors using no bonding wire. This configuration greatly reduces the equivalent electrical distance from the gate electrodes to the lumped capacitor. Therefore, the operating frequency of the large gate width device can be increased to *X*-band or above.

This paper describes the design, fabrication, and microwave performance of a newly developed flip-chip GaAs power FET with an internally matched configuration which is suitable for operation at *X*-band.

II. Fabrication

Fig. 1 shows a scanning-electron microphotograph of the FET chips. The single chip is composed of three unit cells, each of which has twelve gate fingers 200 μm wide and 1 μm long, giving a total gate width W_{gt} of 7.2 mm. Source-to-drain spacing is 4 μm. The distance between the plated posts (gate and drain) and the active area is 160 μm. The chip size is 1.15 mm$\times$0.7 mm.

The fabrication procedures are similar to those for conventional GaAs MESFET's [11]. FET patterns are prepared on epitaxial layer grown on the $\langle 100 \rangle$ oriented Cr-doped substrates by $Ga-AsCl_3-H_2$ vapor transport method. All epitaxial wafers have Fe-doped buffer layers to reduce leak current. Carrier densities of the active layer and the buffer layer are about $1.5-2.5\times10^{17}$ cm^{-3} and $1-10\times10^{12}$ cm^{-3}, respectively. The FET patterns are formed by an ordinary photolithographic lifting technique. The source and drain metallizations consist of multilayers of Au, Ni, and alloyed Au–Ge films. Aluminum gate is formed in a deeply recessed region. The metal layers of Ti, Pt, and Au are formed on the Al gate pad to prevent Al–Au interaction. Gold is electroplated on the source, drain, and gate pads to thickness of 20–30 μm.

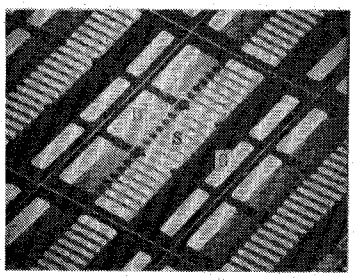

Fig. 1. Scanning-electron microphotograph of the FET chips.

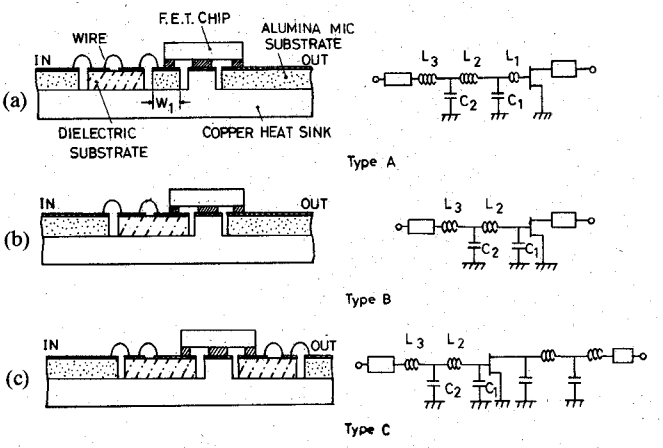

Fig. 2. Cross-sectional views and equivalent circuits of the internally matched flip-chip devices. (a) Gate electrodes are wired to the input lumped capacitor via the alumina ceramic substrate. (b) Gate electrodes are directly connected to the input lumped capacitor. (c) Both the input and output matching networks are made of lumped elements.

Fig. 2(a), 2(b), and 2(c) show cross-sectional views and equivalent circuits of the three fundamental structures, Types A, B, and C of the internally matched flip-chip devices. The chip carrier, which is 8.0 mm long and 5.0 mm wide, consists of the chip mount, the input and output impedance matching networks, and the distributed microstrip lines. Since electroplated source posts are directly bonded to the Au plated Cu heat sink using no bonding wire, small parasitic source inductance and good heat dissipation are realized for all configurations. The lumped capacitors are formed on low loss ($Q>6000$), high dielectric-constant ($\epsilon=41$) substrates with a thickness of 0.4 mm, while the lumped inductances are provided by bonding wires of 25 μm in diameter. The values of these lumped C and L in Fig. 2 are adjusted by changing the area of the capacitors and the number of the wires, respectively. The

maximum capacitance values of the lumped capacitors (C_1 and C_2) formed on the dielectric substrate are restricted by the chip size and the minimum ones by the area necessary for wire bonding. The lumped inductances L_2 and L_3 between the lumped capacitors C_1 and C_2, and between the lumped capacitor C_2 and the distributed microstrip line, respectively, are also restricted by the wire length necessary to bond these lumped elements. Accordingly, we made restrictive conditions for the values of the lumped elements as follows for our present carriers:

$$0.15 \text{ pF} < C_1 \text{ and } C_2 < 7.0 \text{ pF}$$

$$L_2 \text{ and } L_3 < 0.8 \text{ nH}.$$

In Type A, the alumina MIC substrates are arranged at either side of the heat sink. The surface of each is made level with the heat sink. The gate and drain metal posts are also directly bonded to the surfaces of the alumina MIC substrates. The output network is composed of the MIC distributed circuit. The characteristic impedance of the MIC pattern, on which the drain metal posts are attached, is lower than 15 Ω. The input network is composed of the shunt lumped capacitors (C_1 and C_2) formed using a dielectric substrate, the series wire inductance (L_1) between the gate electrodes and the input capacitor (C_1), the series wire inductance (L_2) between lumped capacitors (C_1 and C_2), and the series wire inductance (L_3) between lumped capacitor (C_2) and MIC alumina substrate as shown in Fig. 2(a). The reduction of the series inductance (L_1) in this configuration is limited because the gate electrodes are wired to the input lumped capacitor via the alumina ceramic substrate. The effect of the series inductance (L_1) was investigated by using a carrier with two kinds of the alumina ceramic substrate on which the gate electrodes are attached: one with width W_1 of 0.25 mm and the other of width 0.5 mm. This is because the inductance L_1 corresponds mainly to the width W_1 of the alumina ceramic substrate.

In Type B, the input alumina substrate of width W_1 in Type A is removed and the gate metal posts are directly bonded to the lumped capacitor (C_1) of the dielectric substrate. In this case, the inductance (L_1) between the input lumped capacitor (C_2) and the gate posts can be reduced almost to zero.

In Type C, both the input and output matching networks are made of lumped elements. In comparison with Type B, the output network of Type C can easily match the very low output impedance. The adjustment for large signal matching or for center frequency matching can be realized by changing the number of wires and the capacitor areas individually. For the adjustment of VSWR, L_2 and C_2 were mainly changed, while for center frequency matching, C_1 was adjusted.

The circuit design procedure was based on the small-signal S-parameters of the chip with appropriate modification of the lumped L and C's, taking large-signal effect into account. The input and output impedances of the multichip devices are calculated by extrapolating the S-parameters of the chips with gate widths of 2.4 mm, 4.8 mm, and 7.2 mm, as shown in Fig. 3. The values given have been normalized to the characteristic impedance of 50 Ω. For example, the input and output impedances, Z_{in} and Z_{out}, of the 4-chip device with the gate width of 28.8 mm are estimated to be about $0.3+j6.0$ Ω and $0.8+j9.0$ Ω at 10 GHz, respectively. These extraporations are found to be valid because the matching networks of the multichip devices are well designed using these S-parameters as shown later.

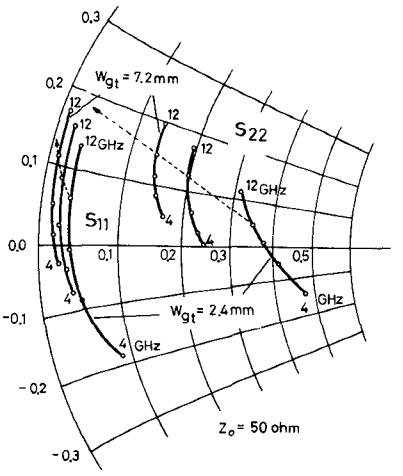

Fig. 3. Typical frequency loci of the input and output impedances for chips with the gate widths of 2.4 mm, 4.8 mm, and 7.2 mm, respectively.

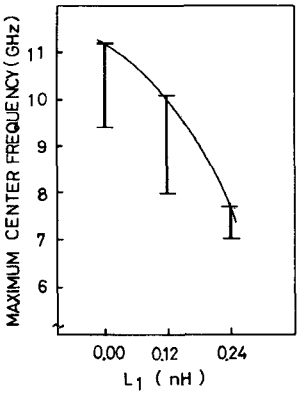

Fig. 4. Maximum center frequency versus series inductance (L_1).

It was ascertained from circuit analysis for the lumped matching networks that the center frequency of the input network most critically depended on the series inductance L_1. The center frequency of the bandwidth in which the internally matched FET actually operates is almost determined by that of the input network. We experimentally investigated the effect of L_1 on the center frequency for the above mentioned three types of the flip-chip configurations in order to find the optimum structure at X-band frequency. The series inductance L_1 in Types B or C is 0.0 nH, and that in Type A having the widths W_1 of 0.25 mm and 0.5 mm are 0.12 nH and 0.24 nH, respectively. Fig. 4 shows the center frequencies of 1-chip devices versus the series inductance L_1, in which the lumped elements except for L_1 are changed so that the FET can operate at as high a frequency as possible in each type. The highest operating

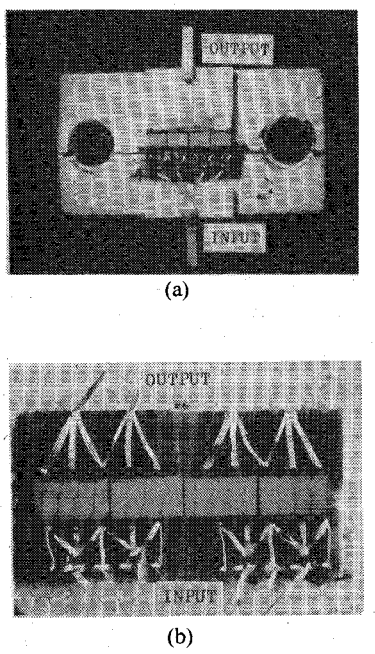

Fig. 5. Top views of internally matched 4-chip devices ($W_{gt}=28.8$ mm) with (a) Type B, and (b) Type C structures.

frequency is designated by f_c and is later called maximum center frequency. It is noted that the maximum center frequency f_c depends strongly on the inductance L_1. The maximum center frequency f_c for the 1-chip device in Type A having W_1 of 0.25 mm is about 10 GHz, while for Types B and C, f_c is about 11 GHz. Based on a circuit simulation for the lumped LC network under the restrictive conditions for the values of the lumped elements, it is calculated that the maximum center frequency of the 4-chip devices is about 10 GHz for both Types B and C, and is about 6.0 GHz for Type A. It is concluded from the results that structures of Types B and C are suitable to internally match the large gate width device at X-band. In this study, the devices with Types B and C structures at the frequency of 10 GHz are mainly discussed.

Fig. 5(a) and 5(b) show top views of internally matched 4-chip devices ($W_{gt}=28.8$ mm) of Types B and C, respectively. Chips to be combined are selected so as to have almost the same values of gate-source breakdown voltage V_{gs0}, pinch-off voltage V_p and drain saturation current I_{dss} in order to achieve the high combining efficiency. The chips are turned over, and the gate, drain, and source metal posts are directly connected by thermocompression bonding. The pressure of the thermocompression bonding is less than 180 kg/cm^2 at 350°C, which causes no serious damage to the devices [12]. For the 4-chip device, no degradation was observed after three cycles of the heat shock test between −60°C and 150°C. The MTTF at 150°C for the 1-chip devices is estimated about 10^8 to 10^9 h from the high temperature storage test. Thermal resistance of the 1-chip device was calculated using an experimentally measured dependence of the gate to source voltage at constant gate current on channel temperature. As thermal resistance for the 1-chip device was about 7°–10°C/W, that for the 4-chip device was speculated to be 2°–3°C/W. Fig. 6

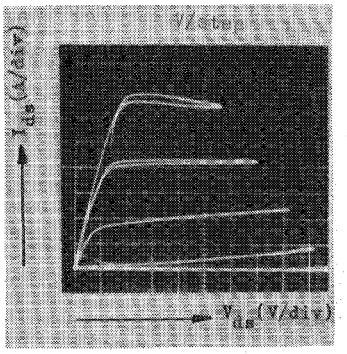

Fig. 6. Typical I–V curve of 4-chip device. (Horizontal: 1 V/div, vertical: 1 A/div, and step: 1 V/step.)

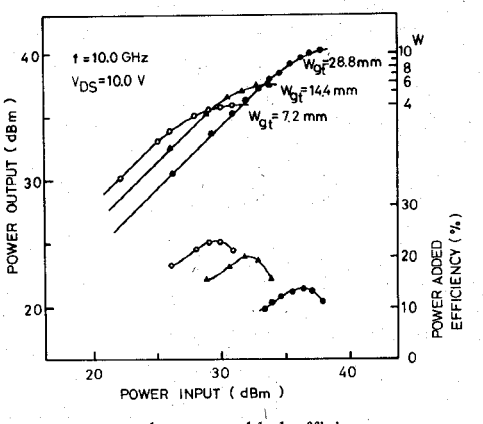

Fig. 7. Power output and power added efficiency versus power input curves for 1-chip ($W_{gt}=7.2$ mm), 2-chip (14.4 mm), and 4-chip (28.8 mm) devices at 10 GHz.

shows a typical I–V curve for the 4-chip device. It displays a saturation current of 7.7 A, pinch-off voltage of 4.0 V and transconductance of 2.6 S.

III. Performance

In the measurement of the input–output power characteristics, MIC 50 Ω test mount was cooled with water for the 4-chip devices and with air for the 1-, 2-, and 3-chip devices. Typical power output versus power input curves for 1-chip ($W_{gt}=7.2$ mm), 2-chip (14.4 mm), and 4-chip (28.8 mm) devices at 10 GHz are shown in Fig. 7 together with the power added efficiencies. The devices are operated at a drain voltage of 10.0 V and a gate voltage of −1.0 V. A 4-chip device gives power output of 10.0 W with 3.0-dB gain, power output at 1-dB gain compression of 9.3 W, saturated power output of 11.5 W with a linear gain of 4.3 dB and power added efficiency of 14.0 percent. A 1-chip device gives a power output at 1-dB gain compression of 3.4 W and saturated power output of 4.0 W. Linear power gain is as high as 8.0 dB. Thus, a power combining efficiency as high as 70 percent was achieved. The saturated power output per unit gate width, P_{sat}/W_{gt}, is 0.55 W/mm for a 1-chip device and 0.4 W/mm for a 4-chip device at 10 GHz.

Fig. 8 shows the power output at 1-dB gain compression $P_{1\,dB}$ and the linear power gain G_{LP} versus the total gate width. In Fig. 8, solid curves and dashed curves correspond to the devices with internal matching circuitry and those

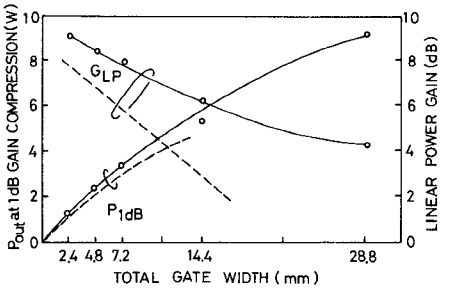

Fig. 8. Power output at 1-dB gain compression and linear power gain at 10 GHz against total gate width, comparing those of the flip-chip devices without the internal matching circuitry.

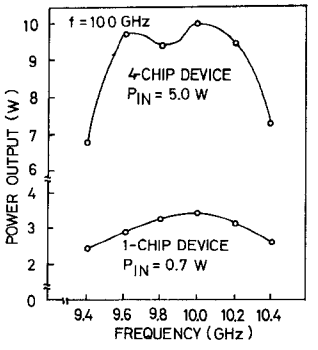

Fig. 9. Frequency response of 4-chip and 1-chip devices with internal matching circuitries.

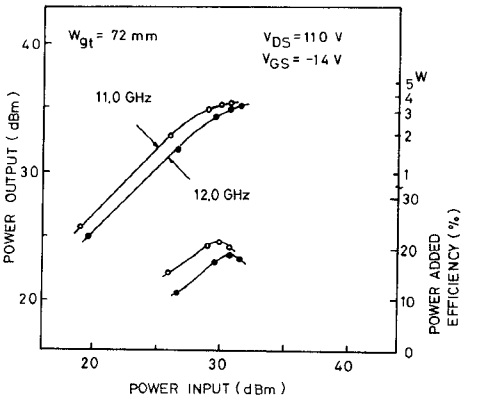

Fig. 10. Typical input–output characteristics of a 1-chip device at 11 GHz and 12 GHz.

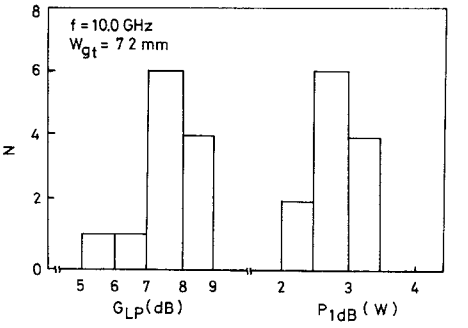

Fig. 11. Distributions of a power gain and a power output at 1-dB gain compression for a 1-chip device at 10-GHz.

without ones, respectively. It is noted that no sudden decrease occurs in power combining efficiency and the linear power gain for internally matched devices with up to a total gate width of 28.8 mm. For example, when the minimum linear power gain required for the device is 4.0 dB at 10 GHz, the internally matched FET can have a gate width three times as wide as that of the device without internal matching circuitry.

Fig. 9 shows the frequency response of the 4-chip and 1-chip devices with internal matching circuitry. The 4-chip device covers 9.5–10.5 GHz with ±0.5-dB gain ripple, while the 1-chip device gives a linear power gain of 6.0 dB in the frequency range from 9.6 GHz to 10.3 GHz with input power of 0.7 W. When the center frequency of a 1-chip device was adjusted to 11 GHz and 12 GHz, the input–output characteristics shown in Fig. 10 were obtained. The 1-chip device gives a linear power gain of 5.3 dB at 12 GHz and 6.6 dB at 11 GHz. The best results obtained are presented in Table I.

Fig. 11 shows the distribution of the power gain G_{LP} and the power output P_{1dB} at 1-dB gain compression of 1-chip devices at 10 GHz for 12 chips randomly selected from three lots which passed dc tests. Narrower distributions both for power gain and power output at 1-dB gain compression are observed. These imply the superior reproducibility of this configuration.

TABLE I
INTERNALLY MATCHED GaAs FLIP-CHIP POWER FET PERFORMANCE

f(GHz)	P_{sat}(W)	P_{1dB}(W)	G_{LP}(dB)	η_{add}(%)	W_{GT}(mm)
10.0	11.5	9.3	4.3	14	28.8
10.0	5.8	5.3	6.3	20	14.4
10.0	4.0	3.4	8.0	23	7.2
10.0	2.6	2.4	8.4	28	4.8
12.0	3.5	3.0	5.3	19	7.2

IV. CONCLUSION

An output of 10 W at 10 GHz was achieved with a newly developed internally matched configuration for flip-chip GaAs power FET's. In this configuration, the gate and drain electrodes are connected directly to the lumped matching capacitors using no bonding wire. These results demonstrate that the internal matching configuration is useful for obtaining high power FET's with sufficient gain in *X*-band.

ACKNOWLEDGMENT

The authors wish to thank Dr. K. Shirahata and Dr. S. Mitsui for their encouragements throughout this work. The authors also wish to express their sincere gratitude to M. Nakatani for his valuable discussions.

REFERENCES

[1] J. V. Dirorenzo and W. R. Wisseman., "GaAs power MESFET's: Design, fabrication, and performance," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 367–378, May 1979.
[2] M. Nakatani, Y. Kadowaki, and T. Ishii., "A 12-GHz 1-W GaAs

MESFET Amplifier," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 1066–1070, Dec. 1979.
[3] P. T. Ho, C. M. Pham, and R. L. Mencik., "A 10-watt, C-band FET amplifier for TWTA replacement," in *1979 IEEE MTT-S Int. Microwave Symp. Dig.*, (Florida), May 1979.
[4] M. Fukuta, T. Mimura, H. Suzuki, and K. Suyama., "4-GHz 15-W Power GaAs MESFET," *IEEE Trans. Electron Devices*, vol. ED-25, pp. 559–562, June 1978.
[5] F. Hasegawa, Y. Takayama, A. Higashisaka, T. Furutsuka, and K. Honjo., "GaAs power MESFETs with a simplified recess structure," in *ISSCC Tech. Dig.*, Feb. 1978, pp. 118–119.
[6] K. Honjo, Y. Takayama, and A. Higashisaka., "High power broadband internal matching technique for microwave GaAs FETs," *Tech. Rep. IECE*, vol. 79, no. 213, ED79–96, Jan. 1980.
[7] S. H. Wemple, W. C. Niehaus, W. O. Schlosser, J. V. Dirolenzo, and H. M. Cox., "Performance of GaAs power MESFETs," *Electron. Lett.*, vol. 14, pp. 175–176, Mar. 1978.
[8] I. Drukier, R. Camisa, S. Jolly, H. Huang, and S. Narayan., "Medium power GaAs field-effect transistors," *Electron. Lett.*, vol. 11, pp. 104–105, Mar. 1975.
[9] Y. Mitsui, M. Kobiki, M. Wataze, M. Otsubo, T. Ishii, and S. Mitsui., "Flip-chip mounted GaAs power f.e.t. with improved performance in *X*- to *Ku*-band," *Electron. Lett.*, vol. 15, pp. 461–462, July 1979.
[10] Y. Takayama, K. Honjo, A. Higashisaka, and F. Hasegawa., "Internally matched microwave broadband linear power FET," in *1977 ISSCC Dig. Tech. Pap.*, pp. 166–167, Feb. 1977.
[11] M. Wataze, Y. Mitsui, T. Shimanoe, M. Nakatani, and S. Mitsui., "High power GaAs f.e.t. prepared by molecular beam epitaxy," *Electron. Lett.*, vol. 14, pp. 759–761 Nov. 1978.
[12] T. Suzuki, M. Nishihata, M. Itoh, S. Mitsui, and H. Miki., *Trans. IECE Japan*, 60-C, p. 661, 1977.

K-Band High-Power GaAs FET Amplifiers

JUN'ICHI SONE AND YOICHIRO TAKAYAMA, MEMBER, IEEE

Abstract—**Lumped-element internal matching techniques were successfully adopted for *K*-band power GaAs FET amplifiers. The developed 18-GHz band two-stage amplifier provides 1.05-W power output at 1-dB gain compression and 1.26-W saturated power output with 8.1-dB small-signal gain. The 20-GHz band single-stage amplifier has 1.04-W power output with 3-dB associated gain. Lumped-element internal matching circuit design as well as amplifier fabrication are described. Intermodulation distortion and AM-to-PM conversion characteristics are also presented.**

I. INTRODUCTION

POWER-OUTPUT CAPABILITY for GaAs FET's has been steadily increasing. Single-stage and multistage amplifiers have already exceeded the 10-W output power level in *C*-band [1] and have exhibited multiwatt capability in *X*-band [2], [3]–[5]. Recently, in *Ku*-band high-power FET's which demonstrate 2-W output power capability have been developed [6]–[8]. High-power amplifier development in *Ku*-band and even in *K*-band, using these FET's, is now expected [6].

Above *Ku*-band, high-power FET chip width becomes comparable to the signal wavelength in a distributed-element microstrip matching circuit and it becomes much more difficult to feed a microwave signal uniformly to such a large transistor. Various parasitic reactances accompanied with FET-to-external circuit connection become appreciable and make wide-band operation of the power FET's difficult to achieve. These problems make usual distributed-element matching techniques, which were successfully used for low-noise GaAs FET amplifiers in *Ku*-, *K*-, and even *Ka*-bands [9], [10], inapplicable to high-power GaAs FET's with extremely low input impedances. These have restricted the use of GaAs FET amplifiers in *Ku*- and *K*-bands.

This paper presents effective application of lumped-element internal matching techniques to *K*-band power GaAs FET amplifiers, and microwave performances of 18- and 20-GHz band high-power FET amplifiers developed using the internal matching techniques. The developed 18-GHz band single-stage amplifier provides 1.25-W power output with 3-dB associated gain. The 20-GHz band single-stage amplifier has 1.04-W power output with 3-dB associated gain. The 18-GHz band two-stage amplifier provides 1.05-W power output at 1-dB gain compression with 8.1-dB small-signal gain and 1.25-W saturated power output.

In Section II, the device structure of NE869 series GaAs FET's and FET small-signal impedances in *K*-band are described. In Section III, lumped-element internal matching circuit design is discussed, as are amplifier fabrication and large-signal tuning. Microwave performances for the developed *K*-band single-stage and two-stage amplifiers are presented in Section IV. The effectiveness of the lumped-element internal matching techniques for FET high-power operation is demonstrated. Finally, in Section V, nonlinear distortion characteristics for the two-stage FET amplifier are discussed.

Manuscript received May 21, 1980; revised December 2, 1980. A condensed version of this paper has been presented at the 1980 IEEE-MTT-S International Microwave Symposium, Washington, D.C.

The authors are with Basic Technology Research Laboratories, Nippon Electric Company, Ltd., Miyazaki, Takatsu-ku, Kawasaki, Japan.

0018-9480/81/0400-0309$00.75 ©1981 IEEE